

14 On page 2 of the Office Action, claims 18-37 are rejected under 35
 15 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,677,224 (Kadosh).
 16 The Examiner states:

17 Kadosh et al. shows (FIG. 1U) a semi-conductor
 18 device including a plurality of field effect transistors,
 19 each transistor comprising a gate (130) over a
 20 channel and a deep source (206) and drain (198)
 21 region with dopants of a first conductivity type (P).
 22 Source (204) and drain (152) extension regions are
 23 integral with the deep source and drain regions,
 24 respectively. The source extension is more heavily
 25 doped (P +) than the drain extension (P-). Kadosh
 26 shows all of the elements of the claims except the
 27 drain extension being deeper than the source
 28 extension. Kadosh does disclose that the source
 29 extension is deeper than the drain extension such
 30 that the device has a low source-drain series
 31 resistance and reduced hot carrier effects.
 32 Therefore, it would have been an obvious
 33 modification to one of ordinary skill in the art to
 34 form the drain extension deeper than the source
 35 extension to lower the drain-source series resistance
 36 since a drain and source are made of the same
 37 materials and only differ because of biasing of the
 38 circuit. With respect to the limitations of the claims
 39 concerning the specific depth and concentration of
 40 the dopants, it would have been obvious to one of
 41 ordinary skill in the art at the time the invention was
 42 made to form the dopants at a specific depth and
 43 concentration, since it has been held that
 44 discovering an optimum value of a result effective
 45 variable involves only routine skill in the art.

46 Applicant respectfully traverses the rejection. Kadosh is referred to below as
 47 the cited art.

48 Applicant respectfully traverses the Examiner's contention that "it would
 49 have been an obvious modification to one of ordinary skill in the art to form the
 50 drain extension deeper than the source extension." The Examiner's contention
 51 is rooted in a belief that the source and drain region are interchangeable.

52 Contrary to the Examiner's contention, the source and drain are the
 53 distinct structures which have established meanings to one of ordinary skill in
 54 the art. Applicant notes that the IEEE Standard Dictionary of Electrical and

55 Electronics Terms defines the drain as "a region in the device structure of an
56 insulated-gate-field-effect transistor (IGFET) which contains a terminal into
57 which charge carriers flow from the source through the channel. It has the
58 potential which is more attractive than the source for the carriers in the
59 channel." Applicant also notes that the IEEE Standard Dictionary of Electrical
60 and Electronic Terms defines the source as "region in the device structure of an
61 insulated-gate-field-effect transistor (IGFET) which contains the terminal from
62 which charged carrier flow into channel toward the drain. It has the potential
63 which is less attractive than the drain for the carriers in the channel."
64 Therefore, the source and drain have completely distinct functions during the
65 operation of a transistor. In fact, the drain and source have opposite functions
66 as one is a supplier of charge carriers and the other is a receiver of charge
67 carriers. Accordingly, when the invention is related to the specific function of
68 the source and drain, the distinction between the source and drain cannot be
69 ignored.

70 Each of independent claims 18, 21, and 31 recites a feature in which the
71 drain extension is deeper than the source extension. This structure provides
72 significant advantages. More particularly, the shallower source extension and
73 deeper drain extension achieves at least three beneficial effects: 1. Substantial
74 immunity to short channel effects; 2. reduced peak electric field in the channel
75 region reduced possibility of hot-carrier injection into the gate oxide; and 3.
76 higher drive current. See present application, page 3, lines 1-10. The shallower
77 source extension allows the transistor to achieve control of short channel
78 effects and higher drive currents and yet the deeper drain extension allows the
79 transistor to reduce hot carrier injection stress. See present application, page 5,
80 line 15 – page 6 – line 7.

81 Kadosh does not disclose or suggest the structure recited cited in
82 independent claims 18, 21 and 31. Indeed, Kadosh shows a drain extension
83 which is shallower than the source extension. There is no suggestion in Kadosh
84 to exchange the source extension with the drain extension. Not only does
85 Kadosh not provide a suggestion for the structure in the present application, it

86 teaches precisely the opposite structure. Therefore, claim 18 and its dependent
87 claims 19-20, claim 21 and its dependent claims 22-30 and claim 31 and its
88 dependent claims 32-37 are patentable over the cited art.

89 As shown in Figure IU, both transistors of Kadosh have a drain extension
90 that is shallower than the source extension. There is clearly no suggestion for
91 the opposite structure recited in the claims 18, 21 and 31 because no where in
92 Kadosh does it mention that the source and the drain extension are
93 interchangeable. Indeed, the specification of Kadosh lists a myriad of
94 alternatives and not one of the alternatives mentions a substitution of the drain
95 extension and the source extension. Kadosh, Col. 10, lines 4-60. Accordingly,
96 claim 18 and its dependent claims 19-20, claim 21 and its dependent claims 22-
97 30 and claim 31 and its dependent claims 32-37 are patentable over the cited
98 art.

99 Further, although Kadosh mentions the advantages of lower source drain
100 resistance and reduced hot carrier effects, it achieves these advantages by
101 relying on a structure with a lightly doped drain, a heavily doped deep drain and
102 ultra-heavily doped deep source. Kadosh, Col. 3, lines 9-15. If one of ordinary
103 skill in the art used Kadosh in pursuit of the advantages mentioned by the
104 Examiner, that person would fabricate an asymmetric transistor with a heavily
105 doped deep drain and an ultra-heavily doped deep source. Reducing the depth
106 of source extension would not even be considered, especially when Kadosh
107 clearly shows a deeper drain extension. Accordingly, claim 18 and its
108 dependent claims 19-20, claim 21 and its dependent claims 22-30 and claim 31
109 and its dependent claims 32-37 are patentable over the cited art.

110 Yet further, rather than relying on ultra-heavy doping of a deep source
111 region, the transistor recited in independent claims 18, 21, and 31 achieves
112 significant advantages with a more elegant structure, a shallower source
113 extension and a deeper drain extension. Achieving advantages with a structure
114 of reduced complexity is strong indicia of nonobviousness. Accordingly, claim
115 18 and its dependent claims 19-20, claim 21 and its dependent claims 22-30
116 and claim 31 and its dependent claims 32-37 are patentable over the cited art.

117 Further, dependent claims 19 and 20 recite a feature wherein the source
118 extension is more heavily doped than the drain extension. Assuming for the
119 sake of argument only that the Examiner's contention the source and drain
120 extension are readily interchangeable to meet the limitations in the claims of the
121 present application, Kadosh would disclose the opposite structure as claimed in
122 claim 19. In claim 19, the source extension, the shallower extension, is more
123 heavily doped than the drain extension, the deeper extension. In contrast,
124 Kadosh clearly shows that the deeper extension is more heavily doped. The
125 Examiner must provide a suggestion in Kadosh to make the shallower extension
126 more heavily doped, especially since such a feature is in contrast to
127 conventional wisdom in which deeper exteriors are more heavily doped.
128 Therefore, Kadosh clearly is teaching the opposite of the structure recited in
129 claims 19 and 20. Accordingly, claims 19 and 20 are additionally patentable
130 over the cited art.

131 With respect to dependent claim 26, the ratio of dopants between the
132 source extension and the drain extension is recited as being approximately five.
133 In contrast, Kadosh discloses a concentration of ratio of 10 to 100 times. See
134 Kadosh, Col. 3, lines 29-33. Clearly, the ratio of doping is different than that as
135 claimed in dependent claim 26. Further, there is no suggestion to reduce the
136 doping ratio of Kadosh by $\frac{1}{2}$ or less. Accordingly, it is respectfully submitted
137 that claim 26 is patentable over the cited art.

138 Further, claim 36 has been amended to recite the unique concentration
139 of dopants associated with the deep source and drain regions and the source
140 extension and the drain extension. As discussed above, Kadosh teaches the
141 use of a deep source region having a different concentration of dopants than the
142 deep drain region and the deep source region having a higher concentration of
143 dopants than the drain extension. In contrast, claim 36 recites that the deep
144 source and drain regions have the same dopant concentrations. Further, the
145 range of concentrations recited in claim 36 for the deep source extension is
146 outside of the range disclosed in Kadosh. There is simply no suggestion for

147 altering the concentration of dopants in Kadosh to meet the limitations of claim
148 36. Accordingly, claim 36 is patentable over Kadosh.

149 Applicant believes that the present application is now in condition for
150 allowance. Favorable reconsideration of the application as amended is
151 respectfully requested. The Examiner is invited to contact the undersigned by
152 telephone if it is felt that a telephone interview would advance the prosecution
153 of the present application.

Respectfully submitted,

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VERSION WITH MARKINGS SHOWING CHANGES

31. An ultra-large scale integrated circuit including a plurality of field effect transistors, the field effect transistors comprising:

a gate structure on a top surface of a semiconductor substrate;

a source extension with dopants of a first conductivity type;

a drain extension with dopants of the first conductivity type; and

[forming] deep source and drain regions with dopants of the first conductivity type, wherein the gate structure is between the source and drain regions, wherein the drain extension is deeper than the source extension.

32. The integrated circuit of claim 31, [wherein the forming source and drain regions] further comprising [comprises]:

[providing] a pair of spacers abutting lateral sides of the gate structure[; and

providing a deep source/drain implant at the source location and the drain location].

36. The integrated circuit of claim 31, wherein the [first conductivity type is N-type] deep source and deep drain regions have a concentration of dopants between 10^{19} and 10^{20} dopants per cc, the source extension has a concentration of dopants between 5×10^{19} and 10^{20} dopants per cc, and the drain extension has a concentration of dopants between 1×10^{19} and 5×10^{19} dopants.

37. The integrated circuit of claim 31, wherein the first conductivity type is P-type or N-type.